

Test Insight Addresses Improved Design-for-Test Flow with Cadence

Integrated Test Flow Uses Cadence Design Data to Debug Test Programs before Silicon is Available

TEL AVIV, Israel—(BUSINESS WIRE)—March 7, 2006— Test Insight, the leading provider of software solutions for the design to test field in the semiconductor industry today announced a validated flow between Virtual Test Wizard and Cadence® Encounter® Test from Cadence Design Systems Inc.

Test insight's Virtual Test Wizard enables customers working on SoCs to identify shortcomings in the chip design and defects in the DUT (Device Under Test) test program early in the design cycle when they can be remedied easily and with minimum expense.

The Test Insight and Cadence joint flow enables users to develop and debug their ATE (Automatic Test Equipment) program in a software-only environment before prototype silicon is available. Virtual Test Wizard emulates the tester's environment with the DUT model output from Cadence Encounter Test.

Virtual Test Wizard methodology advances much of the ATE debug phase to an earlier stage in the project and moves it from very expensive and often difficult to access ATE systems to the convenience of the engineer's desk. This validated flow substantially improves test program quality and shortens the time to tested parts. The joint flow was developed through Test Insight's membership in the Cadence Connections program, which fosters interoperability between Cadence technologies and those of its partners.

Collaboration between Design and Test Made Easier with Virtual Test Wizard

Virtual Test Wizard stands out in delivering a sophisticated solution to efficiently debug test programs before silicon production. Customer experience demonstrates that the joint flow of Virtual Test Wizard and Cadence Encounter Test provides the end user with an improved, quick link to the target tester.

"Cadence Encounter Test customers will find adopting Virtual Test Wizard enables their engineers working on Test Development to start program debug much earlier in the design cycle," says Dima Angert, architecture engineer at Test Insight. "This gives them many significant advantages - it builds better working relationships with the designers, it is easier to make modifications to the design that have significant benefits for test, and it greatly reduces the amount of time required on the ATE with first silicon."

Improved Delay Tests Improve Product Quality

Cadence Encounter True-Time Test is the industry's first delay test ATPG that uses actual post layout design timing information and the specification of the tester's timing capabilities to automatically generate faster-than-at-speed delay tests in a single pass.

"Encounter True-Time Test addresses the challenge to product quality at 90 nanometers, where subtle design-process interactions manifest as delay defects and avoid detections with traditional delay testing," said Sanjiv Taneja, vice-president, Encounter Test at Cadence. "Working with Test Insight enables our joint customers to take advantage of the industry's most advanced ATPG tools."

Test Insight's Wave Wizard and Virtual Test wizard failure logs are validated to assure their compatibility with Encounter Diagnostics' Chip Pad Pattern (CPP) format.

About Test Insight

Test Insight, a standard leader in providing software solutions for the design-for-test field worldwide, delivers innovative, cutting-edge software products that enable acceleration of creation and debug of ATE programs. Leading ATE suppliers and users of both ATE and EDA environments use Test Insight products to bring forward the availability of tested integrated circuits and to improve the production yield of complex digital integrated circuits. Headquartered in Tel Aviv, Israel the company markets its tools through distribution channels and partnership arrangements with ATE and EDA suppliers. For further information about Test Insight and its products, visit www.testinsight.com or contact info@testinsight.com

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